REDUCING CYCLE TIME IN A MEMORY DEVICE

ABSTRACT OF THE DISCLOSURE

A memory device includes a memory cell array, an addressing circuit, a data communication circuit and a control circuit. The addressing circuit receives first signals that are indicative of an address associated with a write command, decodes the address to provide column select signals that are indicative of a column address in the memory cell array, and uses the column address to perform a column redundancy check. The data communication circuit latches data signals that are associated with the write command in response to a data strobe signal. The control circuit causes the addressing circuit to perform the column redundancy check during a delay to accommodate variations in the timing of the data strobe signal and begins providing the column select signals to the memory cell array after performing the column redundancy check. The memory device may be a double data rate (DDR) synchronous dynamic random access memory (SDRAM), for example.